

Figure 1

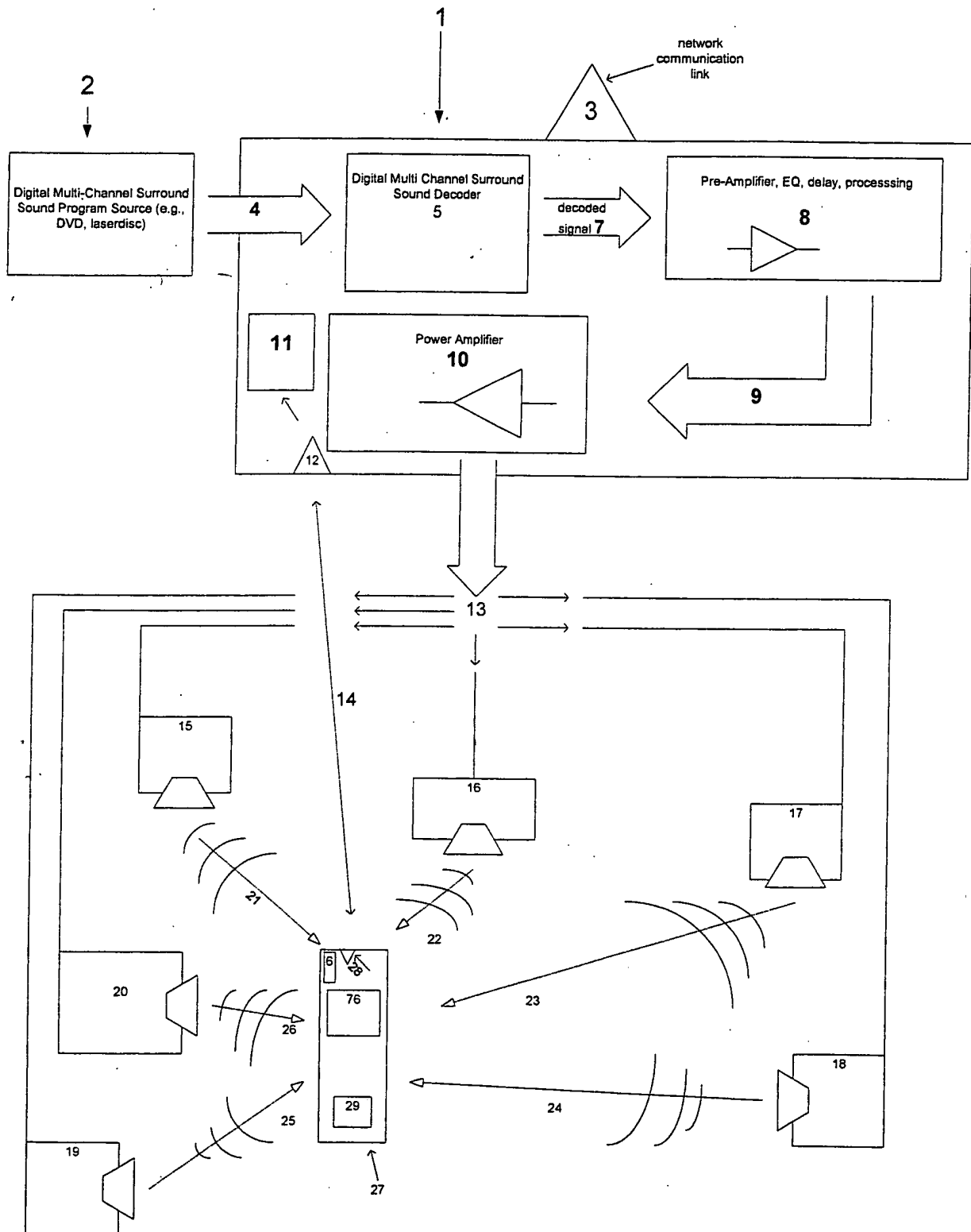


Figure 2

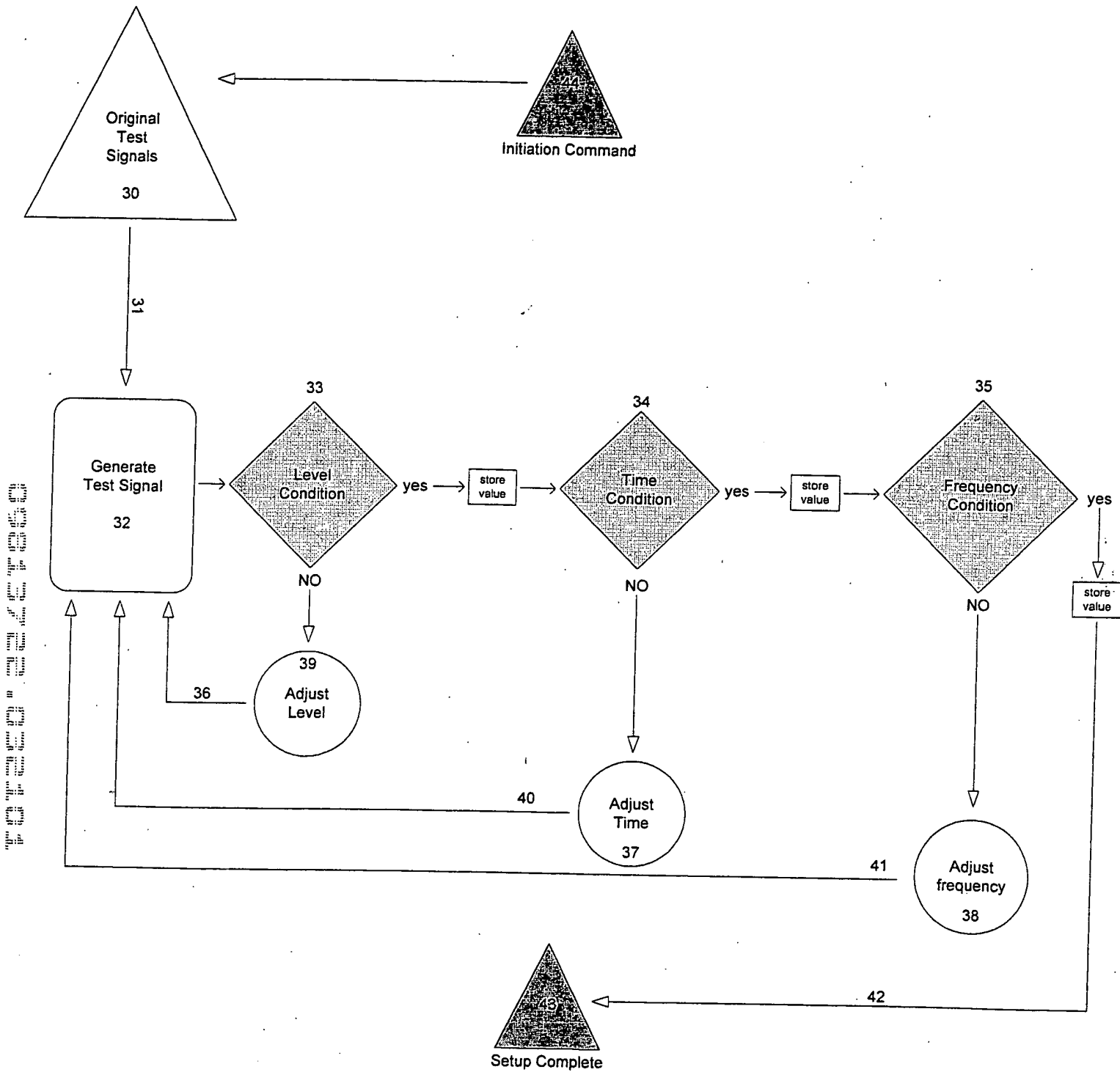


Figure 3

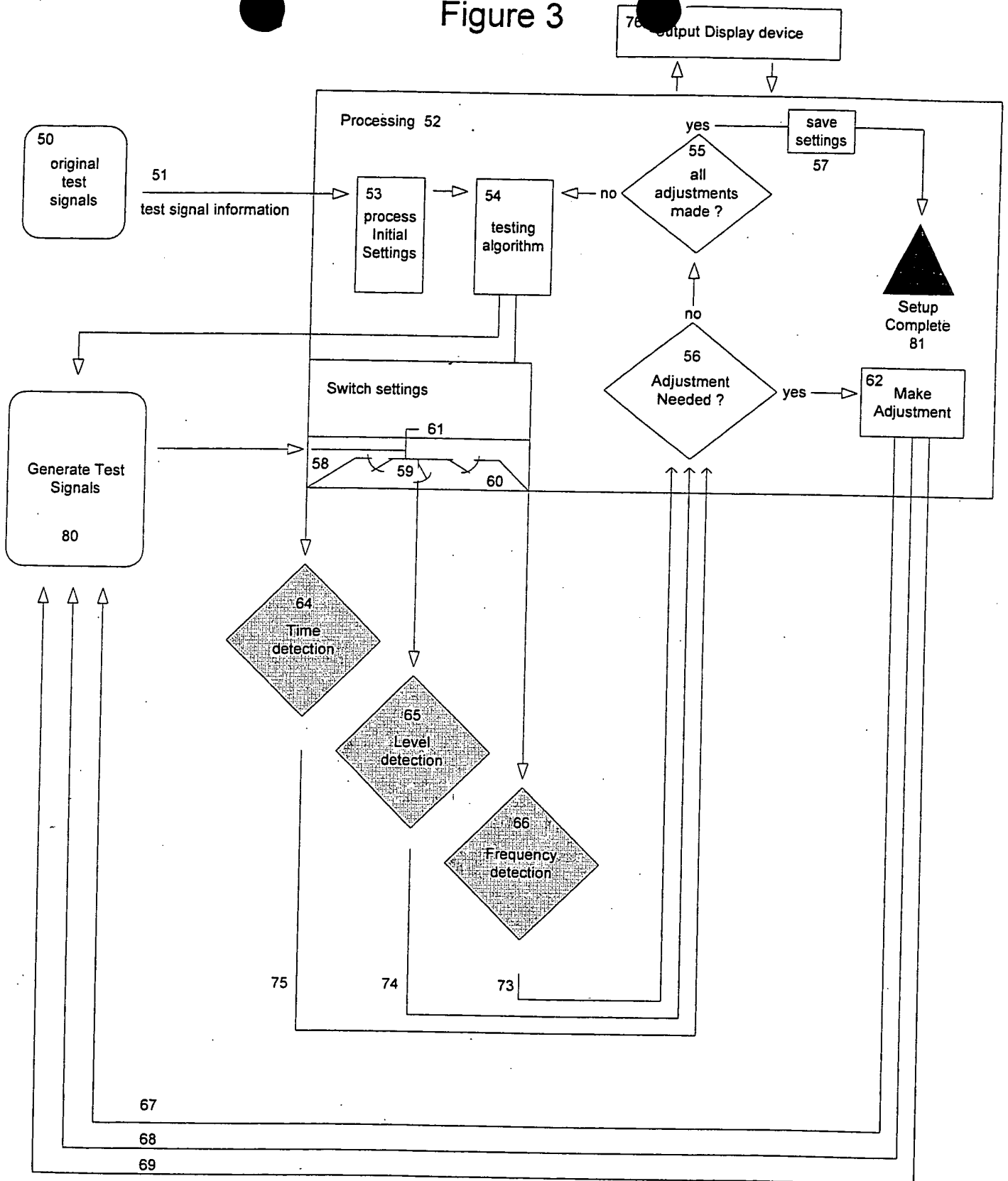


Figure 4

Figure 4 is a block diagram of a system for processing test signals. The system includes a 'Generate Test Signals' block (80) that receives input from 'original test signals' (50) via 'test signal information' (51). The generated signals are sent to a 'Switch settings' block (60) which has multiple outputs (58, 59, 61, 92, 93). These outputs feed into a series of detection blocks: 'Time detection' (64), 'Level Detection' (65), 'Frequency Detection' (66), 'Frequency Center' (90), and 'Frequency Bandwidth' (91). Each detection block outputs a signal (75, 74, 73, 94, 95) to a 'Make Adjustment' block (62). The 'Make Adjustment' block then feeds into a 'Save settings' block (57) and a decision block (55) 'all adjustments made?'. If not all adjustments are made, the system loops back to the 'testing algorithm' (54) via a 'no' path. If all adjustments are made, the system proceeds to 'Setup Complete' (81) and then to the 'output Display device' (76). The 'output Display device' (76) also provides feedback to the 'original test signals' (50) via a 'yes' path.

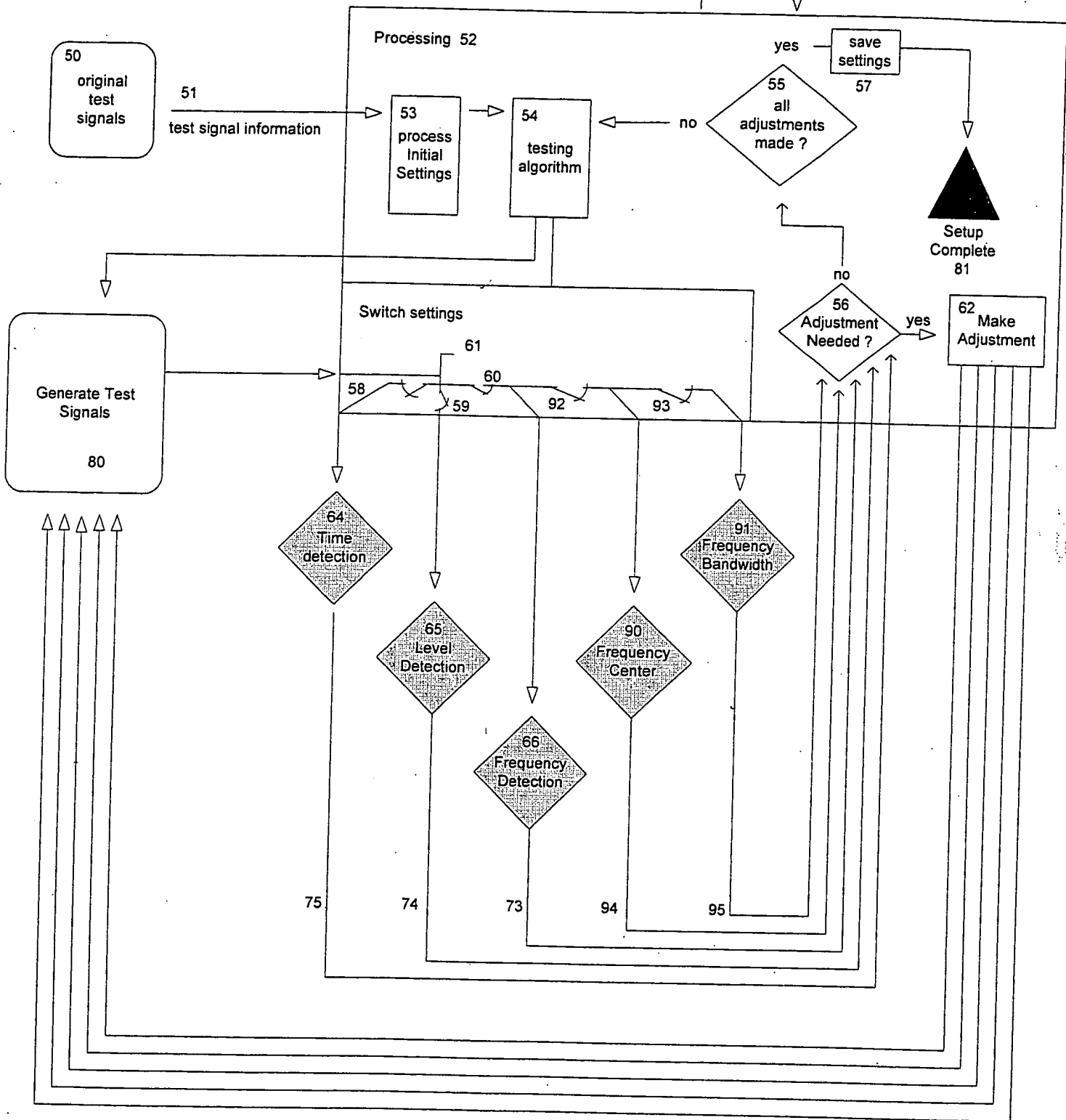


Figure 5

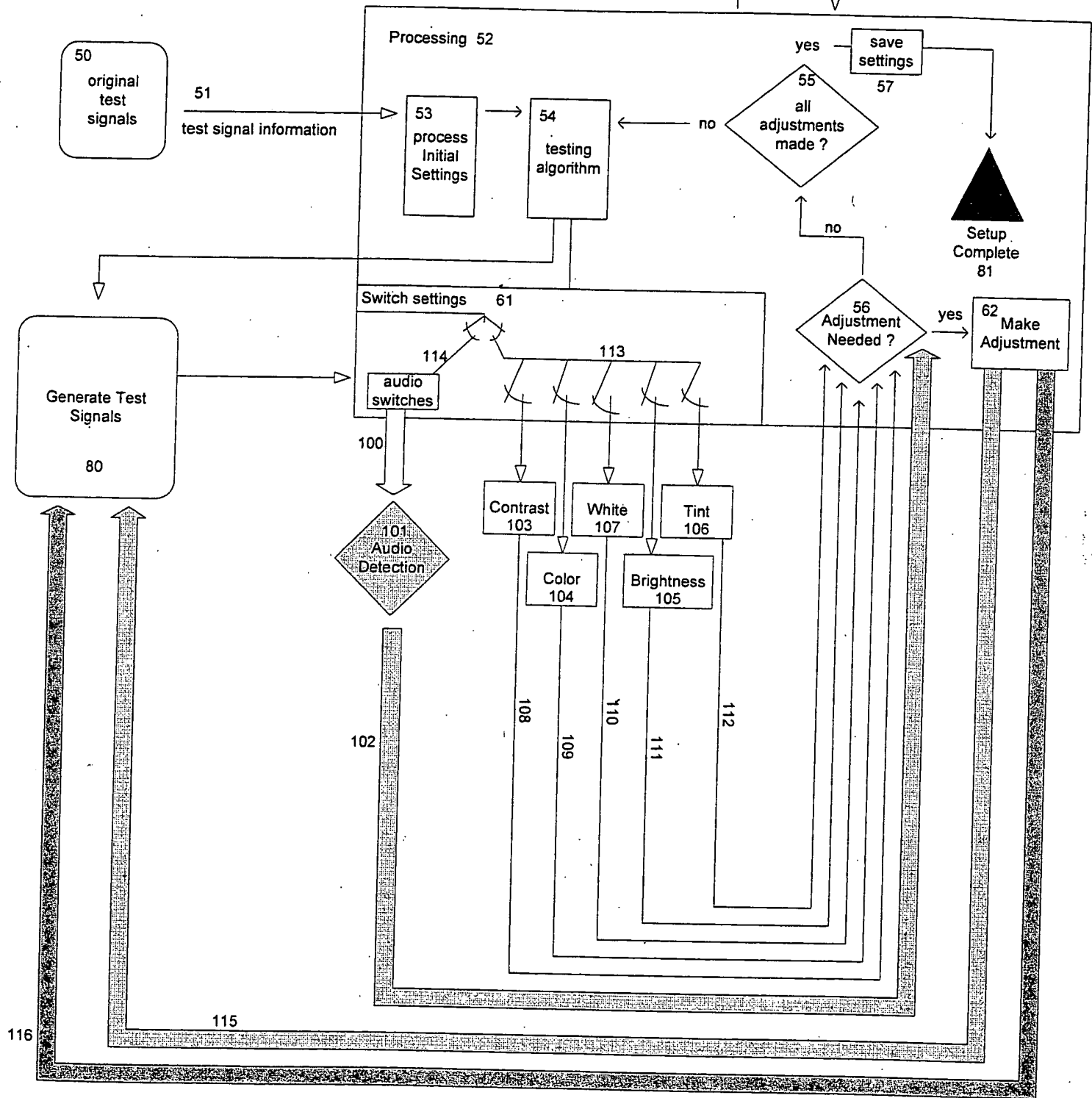


Figure 6

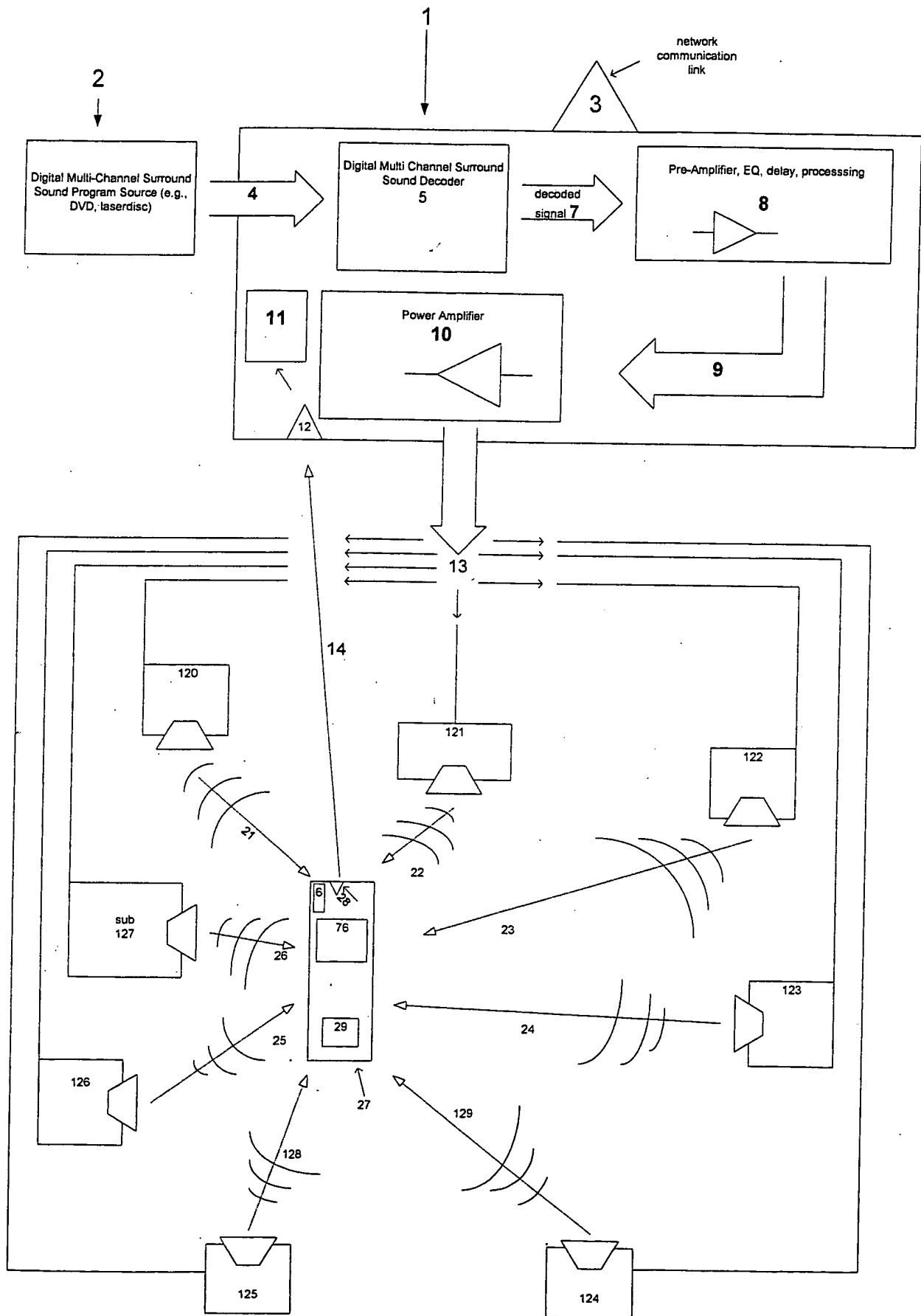


Figure 7

